REMARKS

Claims 1-28 were pending in the Application. Claims 1-6 and 12-17 are rejected under 35 U.S.C. §102(e). Claims 7-10 and 18-21 are rejected under 35 U.S.C. §103(a). Claims 11 and 22 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Claims 23-28 are allowed.

Applicants cancelled claims 1 and 12 without prejudice or disclaimer and reserve the right to file a continuation application to capture the subject matter of cancelled claims 1 and 12. As a result of canceling claims 1 and 12, claims 2-11 and 13-28 are pending in the Application. Applicants note that claims 1 and 12 were cancelled not in light of the cited prior art but to advance prosecution.

Applicants amended claims 2 and 13, as indicated above, to be rewritten in independent form.

Applicants note that claims 2 and 13 were not amended to overcome prior art but to be rewritten in independent form. Hence, no prosecution history estoppel arises from the amendments to claims 2 and 13. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 62 U.S.P.Q.2d 1705, 1711-12 (2002); 56 U.S.P.Q.2d 1865, 1870 (Fed. Cir. 2000). Further, the amendments made to claims 2 and 13 were not made for a substantial reason related to patentability and therefore no prosecution history estoppel arises from such amendments. *See Festo Corp.*, 62 U.S.P.Q.2d 1705 at 1707 (2002); *Warner-Jenkinson Co. v. Hilton Davis Chemical Co.*, 41 U.S.P.Q.2d 1865, 1873 (1997).

Applicants respectfully traverse the rejections to claims 2-11 and 13-28 for at least the reasons stated below and respectfully request that the Examiner reconsider and withdraw these rejections.

I. REJECTIONS UNDER 35 U.S.C. § 102(e):

The Examiner has rejected claims 1-6 and 12-17 under 35 U.S.C. § 102(e) as being anticipated by Solheim et al. (U. S. Patent No. 6,522,671) (hereinafter "Solheim"). Applicants canceled claims 1 and 12 as indicated above and hence the rejections to claims 1 and 12 are moot. Applicants respectfully traverse the rejections to claims 2-6 and 13-17 for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. § 2131.

Applicants respectfully assert that Solheim does not disclose "a control logic unit functionally connected to said port scanning unit for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate" as recited in claim 2 and similarly in claim 13. The Examiner cites element 110 in Figure 2 of Solheim as disclosing a port scanning unit. Office Action (1/26/2006), page 3. The Examiner further cites element 210 as inherently disclosing a control logic unit. Office Action (1/26/2006), page 3. The Examiner further cites element 216 and column 4, lines 10-26 of Solheim as disclosing the above-cited claim limitation. Office Action (1/26/2006), page 3. Applicants respectfully traverse the assertion that Solheim discloses the above-cited claim limitation.

As illustrated in Figure 2 of Solheim, mapping device (element 110) includes frame generation and read logic (element 210). Hence, the mapping device of Solheim (Examiner asserts the mapping device discloses a port scanning unit) includes the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses a control logic unit). Frame generation and read logic is not functionally connected to the mapping. Instead, the frame generation and read logic is part of the mapping device. Hence, Solheim does not disclose a control logic unit functionally connected to a port scanning unit. Thus, Solheim does not disclose all of the limitations of claims 2 and 13, and thus Solheim does not anticipate claims 2 and 13. M.P.E.P. §2131.

Further, Solheim instead discloses that the first and second buffering devices receive the data information D_1, D_2 output from the first and second inputting devices, respectively, and output respective buffered data information to the mapping device (element 110) at outputting periods determined by the mapping device. Column 4, lines 10-15. Solheim further discloses that the percentages of the buffering devices that are filled, hereinafter referred to as the fill levels, are communicated to the mapping device. Column 4, lines 15-18. Solheim further discloses that the mapping device utilizes the fill levels to determine the outputting periods for the buffered data information from the buffering devices and outputs read signals to the buffering devices. Column 4, lines 18-22. There is no language in the cited passage that discloses that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) determines which of the at least two ports need to be handled within which clock cycle. Neither is there any language in the cited passage that discloses that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) determines which of the at least two ports need to be handled within which clock cycle with regard to its input data rate. Thus, Solheim does not disclose all of the limitations of claims 2 and 13, and thus Solheim does not anticipate claims 2 and 13. M.P.E.P. §2131.

Further, Solheim instead discloses a multiplexer (MUX) with a voltage controlled oscillator (VCO) block (element 216) that corresponds to the outputting device mentioned above with reference to FIG. 1. Column 9, lines 1-5. Solheim further discloses that preferably this MUX with VCO block (element 216) is formatted to operate with SONET and so the output bit rate should be 2.5 GHz. Column 9, lines 9-11. There is no language in the description of element 216 that discloses that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) determines which of the at least two ports need to be handled within which clock cycle. Neither is there any language in the description of element 216 that discloses that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) determines which of the at least two ports need to be handled within which clock cycle with regard to its input data rate. Thus, Solheim does not

disclose all of the limitations of claims 2 and 13, and thus Solheim does not anticipate claims 2 and 13. M.P.E.P. §2131.

Applicants further assert that Solheim does not disclose "at least two demultiplexing units for converting said at least two data signals into a parallel data stream of a predetermined width" as recited in claim 4 and similarly in claim 15. The Examiner cites elements 202 and 204 of Solheim as disclosing the above-cited claim limitation. Office Action (1/26/2006), page 4. Applicants respectfully traverse and assert that Solheim instead discloses that the CDR DEMUX devices 202, 204 each receive respective optical input signals and determine the clock rate of the received signal and output the respective clock rate that is synchronous with the respective optical input signals along with n signals that together are a demultiplexed version of the data information to the respective buffering device. Column 5, lines 1-10. There is no language in Solheim that specifically states that the CDR demultiplexing units 202, 204 convert the two input data signals into a parallel data stream of a predetermined width. Thus, Solheim does not disclose all of the limitations of claims 4 and 15, and thus Solheim does not anticipate claims 4 and 15. M.P.E.P. §2131.

Claims 3 and 14 recite the combinations of features of claims 2 and 13, respectively, and thus are not anticipated by Solheim for at least the reasons that claims 2 and 13 are not anticipated by Solheim. Claims 5-6 and 16-17 recite the combinations of claims 4 and 15, respectively, and thus are not anticipated by Solheim for at least the reasons that claims 4 and 15 are not anticipated by Solheim. Claims 3, 5-6, 14 and 16-17 recite additional features which, in combination with the features of the claims upon which they depend, are not anticipated by Solheim.

For example, Applicants further assert that Solheim does not disclose "wherein the control logic unit is configured to control said port scanning unit to access a port having a higher input data rate proportionally more often than a port having a lower input data rate" as recited in claim 3 and similarly in claim 14. As stated above, the Examiner further cites element 210 as inherently disclosing a control logic unit. Office Action (1/26/2006), page 3. The Examine further cites column 4, lines 10-26 and column 7, lines 41-64 of Solheim as disclosing the above-

cited claim limitation. Office Action (1/26/2006), page 3. Applicants respectfully traverse.

Solheim instead discloses that the first and second buffering devices receive the data information D_1, D_2 output from the first and second inputting devices, respectively, and output respective buffered data information to the mapping device (element 110) at outputting periods determined by the mapping device. Column 4, lines 10-15. Solheim further discloses that the percentages of the buffering devices that are filled, hereinafter referred to as the fill levels, are communicated to the mapping device. Column 4, lines 15-18. Solheim further discloses that the mapping device utilizes the fill levels to determine the outputting periods for the buffered data information from the buffering devices and outputs read signals to the buffering devices. Column 4, lines 18-22. Solheim further discloses a frame structure that includes an overhead portion and m frame channels that each comprise N read cycles and one or more stuff bits. Column 7, lines 43-46. Solheim further discloses that the N read cycles within a channel preferably allow for a dynamic bandwidth allocation from the plurality of FIFO memory devices by subdividing the transmission bit rate of the entire frame into N portions that are distributed among the FIFO memory devices. Column 7, lines 46-50. Thus, Solheim discloses a mapping device utilizing the percentages of the buffering devices that are filled to determine the outputting periods for the buffered data information. Solheim further discloses subdividing the transmission bit rate of the entire frame into portions that are distributed among the FIFO memory devices.

There is no language in the cited passages that discloses that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) is configured to control the mapping device (Examiner asserts that the mapping device discloses the port scanning unit) to access a port having a higher input data rate proportionally more often than a port having a lower input data rate. Thus, Solheim does not disclose all of the limitations of claims 3 and 14, and thus Solheim does not anticipate claims 3 and 14. M.P.E.P. §2131.

Applicants further assert that Solheim does not disclose "wherein the storage unit is formed by a FIFO and said FIFO is configured to operate with a speed

corresponding to the input data rate of the connected port" as recited in claim 6 and similarly in claim 17. The Examiner cites elements 206, 208 as disclosing a FIFO storage. Office Action (1/26/2006), page 4. The Examiner further cites element 202 and column 5, lines 1-37 of Solheim as disclosing the above-cited claim limitation. Office Action (1/26/2006), page 4. Applicants respectfully traverse.

Solheim instead discloses that the CDR DEMUX devices 202, 204 each receive respective optical input signals and determine the clock rate of the received signal and output the respective clock rate that is synchronous with the respective optical input signals along with n signals that together are a demultiplexed version of the data information to the respective buffering device. Column 5, lines 1-10. Solheim further discloses that the buffering devices are FIFO memory devices 206, 208. Column 5, lines 10-12. There is no language that the FIFO memory devices (elements 206, 208 of Solheim) are configured to operate with a speed corresponding to the input data rate of the connected port. Solheim simply states that the FIFO memory devices receive the respective clock rate that is synchronous with the respective optical input signals along with n signals that together are a demultiplexed version of the data information. Thus, Solheim does not disclose all of the limitations of claims 6 and 17, and thus Solheim does not anticipate claims 6 and 17. M.P.E.P. §2131.

Further, Applicants do not understand the citing of reference 202 in connection with the rejection of the above-cited claim limitation. Applicants respectfully request the Examiner to particularly point out the significance of element 202 of Solheim in connection with the rejection of the above-cited claim limitation pursuant to 37 C.F.R. §1.104(c)(2). Thus, Solheim does not disclose all of the limitations of claims 6 and 17, and thus Solheim does not anticipate claims 6 and 17. M.P.E.P. §2131.

As a result of the foregoing, Applicants respectfully assert that not each and every claim limitation was found within Solheim, and thus claims 1-6 and 12-17 are not anticipated by Solheim. M.P.E.P. §2131.

II. REJECTIONS UNDER 35 U.S.C. §103(a):

The Examiner has rejected claims 7-10 and 18-21 under 35 U.S.C. §103(a) as being unpatentable over Solheim in view of Goodman (U.S. Patent No. 6,636,529). Applicants respectfully traverse these rejections for at least the reasons stated below and respectfully request the Examiner to reconsider and withdraw these rejections.

A. Solheim and Goodman, taken singly or in combination, do not teach or suggest the following claim limitations.

Applicants respectfully assert that Solheim and Goodman, taken singly or in combination, do not teach or suggest "a central buffer connected to said port scanning unit into which data form all ports are written" as recited in claim 7 and similarly in claim 18. The Examiner cites column 9, line 50 – column 10, line 13 and Figure 14 of Goodman as teaching the above-cited claim limitation. Office Action (1/26/2006), page 6. Applicants respectfully traverse.

Goodman instead teaches a FIFO (element 490) that bridges the domain of the data clock based on the incoming data signal and the SDH container clock. Column 10, lines 2-4. Goodman further teaches that the FIFO receives inter-packet data for retiming. Column 10, lines 1-2. As understood by the Applicants, the Examiner is asserting that FIFO (element 490) is connected to a port scanning unit for storing data from all ports. However, there is no language in Goodman that teaches that the FIFO (element 490) is connected to a port scanning unit configured to extract data from ports providing data streams having at least two different input data rates. Furthermore, there is no language in Goodman that teaches that the FIFO (element 490) receives data from ports. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7 and 18, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Solheim and Goodman, taken singly or in combination, do not teach or suggest "a control logic unit functionally connected to said port scanning unit for determining which of said at least two ports need to be handled within which clock cycle with regard to its input data rate" as recited in claim 8 and similarly in claim 19. The Examiner cites element 110 in Figure 2 of Solheim

as teaching a port scanning unit. Office Action (1/26/2006), page 5. The Examiner further cites element 210 as inherently teaching a control logic unit. Office Action (1/26/2006), page 5. The Examiner further cites element 216 and column 4, lines 10-26 of Solheim as teaching the above-cited claim limitation. Office Action (1/26/2006), page 5. Applicants respectfully traverse the assertion that Solheim teaches the above-cited claim limitation.

As illustrated in Figure 2 of Solheim, mapping device (element 110) includes frame generation and read logic (element 210). Hence, the mapping device of Solheim (Examiner asserts the mapping device discloses a port scanning unit) includes the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses a control logic unit). Frame generation and read logic is not functionally connected to the mapping. Instead, the frame generation and read logic is part of the mapping device. Hence, Solheim does not teach a control logic unit functionally connected to a port scanning unit. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 8 and 19, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Further, Solheim instead teaches that the first and second buffering devices receive the data information D_1, D_2 output from the first and second inputting devices, respectively, and output respective buffered data information to the mapping device (element 110) at outputting periods determined by the mapping device. Column 4, lines 10-15. Solheim further teaches that the percentages of the buffering devices that are filled, hereinafter referred to as the fill levels, are communicated to the mapping device. Column 4, lines 15-18. Solheim further teaches that the mapping device utilizes the fill levels to determine the outputting periods for the buffered data information from the buffering devices and outputs read signals to the buffering devices. Column 4, lines 18-22. There is no language in the cited passage that teaches that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) determines which of the at least two ports need to be handled within which clock cycle. Neither is there any language in the cited passage that teaches that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic

unit) determines which of the at least two ports need to be handled within which clock cycle with regard to its input data rate. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 8 and 19, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Solheim and Goodman, taken singly or in combination, do not teach or suggest "a central buffer connected to said port scanning unit into which data form all ports are written" as recited in claim 8 and similarly in claims 10, 19 and 21. The Examiner cites column 9, line 50 – column 10, line 13 and Figure 14 of Goodman as teaching the above-cited claim limitation. Office Action (1/26/2006), page 6. Applicants respectfully traverse.

Goodman instead teaches a FIFO (element 490) that bridges the domain of the data clock based on the incoming data signal and the SDH container clock. Column 10, lines 2-4. Goodman further teaches that the FIFO receives inter-packet data for retiming. Column 10, lines 1-2. As understood by the Applicants, the Examiner is asserting that FIFO (element 490) is connected to a port scanning unit for storing data from all ports. However, there is no language in Goodman that teaches that the FIFO (element 490) is connected to a port scanning unit configured to extract data from ports providing data streams having at least two different input data rates. Furthermore, there is no language in Goodman that teaches that the FIFO (element 490) receives data from ports. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 8, 10, 19 and 21, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Solheim and Goodman, taken singly or in combination, do not teach or suggest "wherein the control logic unit is configured to control said port scanning unit to read per access from a port having a higher input data rate proportionally more data than from a port having a lower input data rate and writing the data into said central buffer with a single clock speed" as recited in claim 8 and similarly in claim 19. As stated above, the Examiner further cites element 210

as inherently disclosing a control logic unit. Office Action (1/26/2006), page 5. The Examine further cites column 4, lines 10-26 and column 7, lines 41-64 of Solheim as disclosing the above-cited claim limitation. Office Action (1/26/2006), page 5. Applicants respectfully traverse.

Solheim instead teaches that the first and second buffering devices receive the data information D_1, D_2 output from the first and second inputting devices, respectively, and output respective buffered data information to the mapping device (element 110) at outputting periods determined by the mapping device. Column 4, lines 10-15. Solheim further teaches that the percentages of the buffering devices that are filled, hereinafter referred to as the fill levels, are communicated to the mapping device. Column 4, lines 15-18. Solheim further teaches that the mapping device utilizes the fill levels to determine the outputting periods for the buffered data information from the buffering devices and outputs read signals to the buffering devices. Column 4, lines 18-22. Solheim further teaches a frame structure that includes an overhead portion and m frame channels that each comprise N read cycles and one or more stuff bits. Column 7, lines 43-46. Solheim further teaches that the N read cycles within a channel preferably allow for a dynamic bandwidth allocation from the plurality of FIFO memory devices by subdividing the transmission bit rate of the entire frame into N portions that are distributed among the FIFO memory devices. Column 7, lines 46-50. Thus, Solheim teaches a mapping device utilizing the percentages of the buffering devices that are filled to determine the outputting periods for the buffered data information. Solheim further teaches subdividing the transmission bit rate of the entire frame into portions that are distributed among the FIFO memory devices.

There is no language in the cited passages that teaches that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) is configured to control the mapping device (Examiner asserts that the mapping device discloses the port scanning unit) to read per access from a port having a higher input data rate proportionally more data than from a port having a lower input data rate. Neither is there any language in the cited passages that teaches that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) is configured to

control the mapping device (Examiner asserts that the mapping device discloses the port scanning unit) to read per access from a port having a higher input data rate proportionally more data than from a port having a lower input data rate and writing the data into a central buffer with a single clock speed. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 8 and 19, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Applicants further assert that Solheim and Goodman, taken singly or in combination, do not teach or suggest "wherein the control logic unit is configured to control said port scanning unit to read per access from all ports the same amount of data and writing the data from a port having a higher input data rate proportionally more often into said central buffer than from a port having a lower input data rate" as recited in claim 10 and similarly in claim 21. As stated above, the Examiner further cites element 210 as inherently disclosing a control logic unit. Office Action (1/26/2006), page 7. The Examine further cites column 4, lines 10-26 and column 7, lines 41-64 of Solheim as disclosing the above-cited claim limitation. Office Action (1/26/2006), page 7. Applicants respectfully traverse.

Solheim instead teaches that the first and second buffering devices receive the data information D_1, D_2 output from the first and second inputting devices, respectively, and output respective buffered data information to the mapping device (element 110) at outputting periods determined by the mapping device. Column 4, lines 10-15. Solheim further teaches that the percentages of the buffering devices that are filled, hereinafter referred to as the fill levels, are communicated to the mapping device. Column 4, lines 15-18. Solheim further teaches that the mapping device utilizes the fill levels to determine the outputting periods for the buffered data information from the buffering devices and outputs read signals to the buffering devices. Column 4, lines 18-22. Solheim further teaches a frame structure that includes an overhead portion and m frame channels that each comprise N read cycles and one or more stuff bits. Column 7, lines 43-46. Solheim further teaches that the N read cycles within a channel preferably allow for a dynamic bandwidth allocation from the plurality of FIFO memory devices by subdividing the transmission bit rate of the entire frame into N portions that are distributed among the FIFO memory

devices. Column 7, lines 46-50. Thus, Solheim teaches a mapping device utilizing the percentages of the buffering devices that are filled to determine the outputting periods for the buffered data information. Solheim further teaches subdividing the transmission bit rate of the entire frame into portions that are distributed among the FIFO memory devices.

There is no language in the cited passages that teaches that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) is configured to control the mapping device (Examiner asserts that the mapping device discloses the port scanning unit) to read per access from all ports the same amount of data. Neither is there any language in the cited passages that teaches that the frame generation and read logic (Examiner asserts that the frame generation and read logic discloses the control logic unit) is configured to control the mapping device (Examiner asserts that the mapping device discloses the port scanning unit) to read per access from all ports the same amount of data and writing the data from a port having a higher input data rate proportionally more often into the central buffer than from a port having a lower input data rate. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 10 and 21, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Claim 9 recites the combinations of claim 7 or 8, and thus is patentable over Solheim in view of Goodman for at least the reasons that claims 7 and 8 are patentable over Solheim in view of Goodman. Claim 20 recites the combinations of claim 18 or 19, and thus is patentable over Solheim in view of Goodman for at least the reasons that claims 18 and 19 are patentable over Solheim in view of Goodman. Claims 9 and 20 recite additional features which, in combination with the features of the claims upon which it depends, are patentable over Solheim in view of Goodman.

For example, Solheim and Goodman, taken singly or in combination, do not teach or suggest "at least two demultiplexing units associated to each port, whereby the resulting data width of a demultiplexing unit is proportionally larger at a port having a higher input data rate" as recited in claim 9 and similarly in claim 20. The

Examiner cites elements 202, 204 and column 5, lines 1-12 of Solheim as teaching the above-cited claim limitation. Office Action (1/26/2006), page 6. Applicants respectfully traverse.

Solheim instead teaches that the CDR DEMUX devices 202, 204 each receive respective optical input signals and determine the clock rate of the received signal and output the respective clock rate that is synchronous with the respective optical input signals along with n signals that together are a demultiplexed version of the data information to the respective buffering device. Column 5, lines 1-10. Solheim further teaches that the buffering devices are FIFO memory devices 206, 208. Column 5, lines 10-12. Hence, Solheim teaches that the CDR demux devices (elements 202, 204) output the respective clock rate that is synchronous with the respective optical input signals along with n signals that together are a demultiplexed version of the data information to the respective buffering device. There is no language in the cited passage that teaches that the CDR demux devices (elements 202, 204) output the n signals that have a width proportionally larger at a port having a higher input data rate. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 9 and 20, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

As a result of the foregoing, Applicants respectfully assert that there are numerous claim limitations not taught or suggested in Solheim in view of Goodman, and thus the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 7-10 and 18-21. M.P.E.P. §2143.

B. The Examiner has not provided any objective evidence or source of motivation for combining Solheim with Goodman to include the limitations of claims 7-8 and 18-19.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the

patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention may often be found in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that Solheim does not teach have a central buffer connected to a port scanning unit into which data from all ports are written, as recited in claim 7 and similarly in claims 8, 10, 18, 19 and 21. Office Action (1/26/2006), pages 6, 7 and 8. The Examiner's motivation for modifying Solheim with Goodman to have a central buffer connected to a port scanning unit into which data from all ports are written, as recited in claim 7 and similarly in claims 8, 10, 18, 19 and 21, is "to prevent data loss by bridging the clock of incoming signal with the output signal." Office Action (1/26/2006), pages 6 and 8. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

The Examiner has not provided a source for his motivation for modifying Solheim to include the above-cited claim limitation. The Examiner simply states "to prevent data loss by bridging the clock of incoming signal with the output signal" as motivation for modifying Solheim to include the above-cited claim limitation. The motivation to modify Solheim must come from one of three possible sources: the nature of the problem to be solved, the teachings of the prior art, and the knowledge

of persons of ordinary skill in the art. *In re Rouffet*, 149 F.3d 1350, 1357, 47 U.S.P.Q.2d 1453, 1457-48 (Fed. Cir. 1998). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 7, 8, 10, 18, 19 and 21. *Id.*

Furthermore, the Examiner's motivation ("to prevent data loss by bridging the clock of incoming signal with the output signal") does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Solheim to include the above-cited missing claim limitation from claims 7, 8, 10, 18, 19 and 21. According, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 7, 8, 10, 18, 19 and 21. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

Solheim addresses the problem of using a different piece of hardware for each different protocol or set of protocols that are to be combined in connection with an optical fiber communication system. Column 2, lines 3-6. The Examiner has not provided any reasons as to why one skilled in the art would modify Solheim, which overcomes the above-mentioned problem by developing a protocol independent multiplexer that allows for input signals of a variety of different bit rates to be received while outputting a single output with a bit rate that may be different than any of the received signals (column 2, lines 13-17), to have a central buffer connected to a port scanning unit into which data from all ports are written (Examiner admits that Solheim does not teach this limitation). The Examiner's motivation ("to prevent data loss by bridging the clock of incoming signal with the output signal") does not provide such reasoning. That is, the Examiner's motivation does not provide reasons as to why one skilled in the art would modify Solheim, whose purpose is to develop a protocol independent multiplexer that allows for input signals of a variety of different bit rates to be received while outputting a single output, to have a central buffer connected to a port scanning unit into which data from all ports are written. Further, the Examiner has not provided any rationale connection between preventing data loss

(Examiner's motivation) and having a central buffer connected to a port scanning unit into which data from all ports are written (missing claim limitation). The Examiner must provide objective evidence in modifying Solheim to include the above-cited missing limitation of claims 7, 8, 10, 18, 19 and 21. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Instead, the Examiner is merely relying upon his own subjective opinion which is insufficient to support a *prima facie* case of obviousness in rejecting claims 7, 8, 10, 18, 19 and 21. *Id.* Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 7, 8, 10, 18, 19 and 21. *Id.*

III. ALLOWABLE SUBJECT MATTER:

Applicants thank the Examiner for the allowance of claims 23-28 and the indication of allowability of claims 11 and 21.

IV. CONCLUSION

As a result of the foregoing, it is asserted by Applicants that claims 2-11 and 13-28 in the Application are in condition for allowance, and Applicants respectfully request an allowance of such claims. Applicants respectfully request that the Examiner call Applicants' attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

WINSTEAD SECHREST & MINICK P.C.

Attorneys for Applicants

By: _____

Robert A. Voigt, Jr.
Reg. No. 47,159
Kelly K. Kordzik
Reg. No. 36,571

P.O. Box 50784
Dallas, TX 75201
(512) 370-2832

Austin_1 307430v.1